Amendments to the Specification:

Amend page 1, paragraph beginning at line 3, as follows:

The present application relates to patent application serial no. 09/838,395, ~~docket RAL920010017US2~~, "High Speed Network Processor" which is assigned to the assignee of the present invention. The patent application serial no. 09/838,395 "High Speed Network Processor" describes a high performance network processor formed from multiple interconnected chips and is fully incorporated herein by reference.

Amend page 7, paragraph beginning at line 6, as follows:

Still referring to Figure 1, the CSIX interposer interface 28 provides an interface into a switching fabric (not shown). The CSIX is a standard interface implemented in a Field Programmable Gate Array (FPGA). "CSIX" is the acronym used to describe the "Common Switch Interface Consortium". It is an industry group whose mission is to develop common standards for attaching devices like network processors to a switch fabric. Its specifications are ~~publically~~ publicly available at www.csix.org. The "CSIX Interposer FPGA" converts the "SPI-4 Phase-1" bus interface found on the Data Flow Chip into the CSIX switch interface standard defined in the CSIX specifications. This function could also be designed into an ASIC, but it is simple enough that it could be implemented in an FPGA avoiding the cost and complexity of designing and fabricating an ASIC.

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Amend page 10, paragraph beginning at line 16, as follows:

The data flow arbiter 54 provides arbitration for the data flow manager 58, frame alteration 52 and free list manager 60. The data flow manager 58 controls the flow of data between the NP Complex Chip 16 and the Data Flow chip (Figure 1). The free list manager 60 provides the free list of buffers that is available for use. A completion unit 62 is coupled to EPC 44. The completion unit provides the function which ensures that frames leaving the EPC 44 are in the same order as they were received. Enqueue buffer 64 is connected to completion unit 62 and Frame Alteration 52 and queues frames received from the completion unit to be transferred to the Data Flow chip through the Chip to Chip Macro 56. Packet buffer arbiter 66 provides arbitration for access to packet buffer 51. Configuration registers 68 stores information for configuring the chip. An instruction memory 70 stores instructions which are utilized by the EPC 44. Access for boot code in the instruction memory 70 is achieved by the Serial/Parallel Manager (SPM) 72. The SPM loads the initial boot code into the EPC following power-on of the NP Complex Chip.

Amend page 13, paragraph beginning at line 2, as follows:

Control store memory 16' provides large DRAM tables and fast SRAM tables to support wire speed classification of millions of flows. Control store includes two on-chip 3K x 36 SRAMs (H1A and H1B), two on-chip 3K x 128 SRAMs (H0A and H0B), four external 32-bit DDR SDRAMs (D0A, D0B, D1A, and D1B), two external 36-bit ZBT SRAMs (S0A and S0B), and one external 72-bit ZBT SRAM (S1). The 72-bit ZBT SRAM interface may be optionally used for attachment of a contents address memory (CAM) for improved lookup performance. The numerals such as 18, 64, 32, etc. associated with bus for each of the memory elements, in Figure 2 represent the size of the data bus

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interconnecting the respective memory unit to the control store arbiter. For example, 18 besides the bus interconnecting the PowerPC memory D6 to control store arbiter 36 indicates that the data bus is 18 bits wide and so forth for the others.

Amend page 23, paragraph beginning at line 5, as follows:

Still referring to Figure 5, the Chip to Chip Macro 32 and Chip to Chip Macro 124 aggregates all communication between ASIC #1, ASIC #2 onto the single Chip to Chip interface bus 30 that connects the two ASICs. By so doing, the number of I/O pins used to effectuate communication can be significantly reduced. In operation if Macro A1 wishes to communicate with Macro B1, Macro A1 asserts a request signal indicating its desire to communicate with Macro B1. The request is intercepted by Chip to Chip Macro 32 and is formed into a packet of information called a "message" that is interleaved with other requests flowing between macros on ASIC #1 to macros on ASIC #2. An identification called a message ID is ~~preppended~~ preappended to the message that indicates it is targeted for Macro B1. The request message is transferred from Chip to Chip Macro 32 in ASIC #1 to Chip to Chip Macro 124 on ASIC #2 via a high speed bus called Chip to Chip Interface Bus 30. As will be explained subsequently Chip to Chip Interface Bus 30 includes independent transmission busses carrying information between the two ASICs. By way of an example, bus 30' transmits information from Chip to Chip Macro 32 to Chip to Chip Macro 124. Likewise, 30" transports information from Chip to Chip Macro 124 to Chip to Chip Macro 32.. Upon reception of the request message by Chip to Chip Macro 124 on ASIC #2, the message ID is decoded to determine that the request is destined for Macro B1. The Chip to Chip Macro 124 in ASIC #2 then asserts the request to Macro B1 as if it were directly attached to A1. If Macro B1 needs to send a response to the request it uses the same technique to cause the Chip to Chip Macros 32 and 124 to forward a response message back to Macro A1. If no response is required then the operation is

complete. The Chip to Chip Macros 32 and 124 also support requests flowing in the opposite direction (i.e. a request from Macro B1 to Macro A1).

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